



Data Systems  
Technology  
Division  
520

Level 1 Processing  
EOSDIS  
Technology  
Transfer Workshop

# Level One Processing Using Field Programmable Gate Array Technology

**Mark Stephens**  
**System Applications Section, Code 521.2**  
**301 286-4269**  
**[mark.stephens@gsfc.nasa.gov](mailto:mark.stephens@gsfc.nasa.gov)**



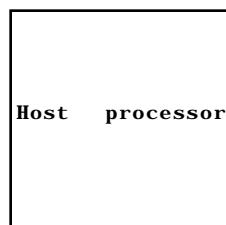
# FPGA Based Co-processor

- Inexpensive host workstations are used with a Field Programmable Gage Array (FPGA) based co-processor board(s)
- Replace time intensive functions with FPGA accelerated versions

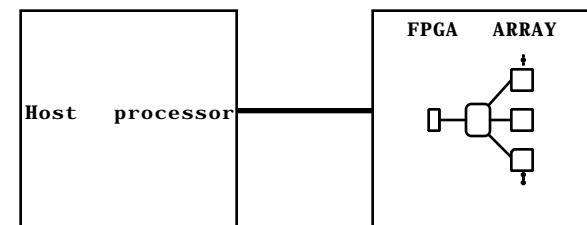
```
main()
{
    initArrays();
    ...
    geometricCorrection( x, y, a, b );
    calibration( x, y, a, b );
}

geometricCorrection( x, y, a, b )
{
    ...
    for( i=0; i<=maxI; i++ )
    {
        y[i] = a[i] * x[i] + b[i-1] * y[i-1] + b[i-2] * y[i-2];
    }
    ...
}

calibration( x, y, a, b )
{
    ...
}
```



```
main()
{
    initArrays();
    ...
    // Read files of configuration bit streams into processor RAM
    loadConfigToRAM( geoCorrectConfig, "geoCorr.config");
    loadConfigToRAM( calibrationConfig, "calCorr.config");
    ...
    // Program FPGA arrays with first configuration bit stream
    arrayLoadConfig( geoCorrectConfig );
    ...
    // Pipeline data thru arrays
    arrayPipeline( x, y, a, b );
    ...
    // Program FPGA arrays with next configuration bit stream
    arrayLoadConfig( calibrationConfig );
    arrayPipeline( x, y, a, b );
    ...
}
```





# Example of Speed Enhancements

- Parallelism, pipelined data and Direct Memory Access (DMA) account for much of the acceleration
- CPUs typically have a three cycle instruction execution speed: fetch->decode address->execute.  
Hardware implementation have a load data (DMA)->execute

Speed enhancements for equation:

$$y[i] = a[i] * x[i] + b[i - 1] * y[i - 1] + b[i - 2] * y[i - 2]$$

Using reverse polish notation:

Sequential computer

In "hardware"

a[i]		a[i]*x[i]	b[i - 1]*y[i - 1]	b[i - 2]*y[i - 2]
x[i]			+	
*				+ -> y[i]
b[i - 1]				
y[i - 1]				
*				
+				
b[i - 2]				
y[i - 2]				
*				
+ -> y[i]				

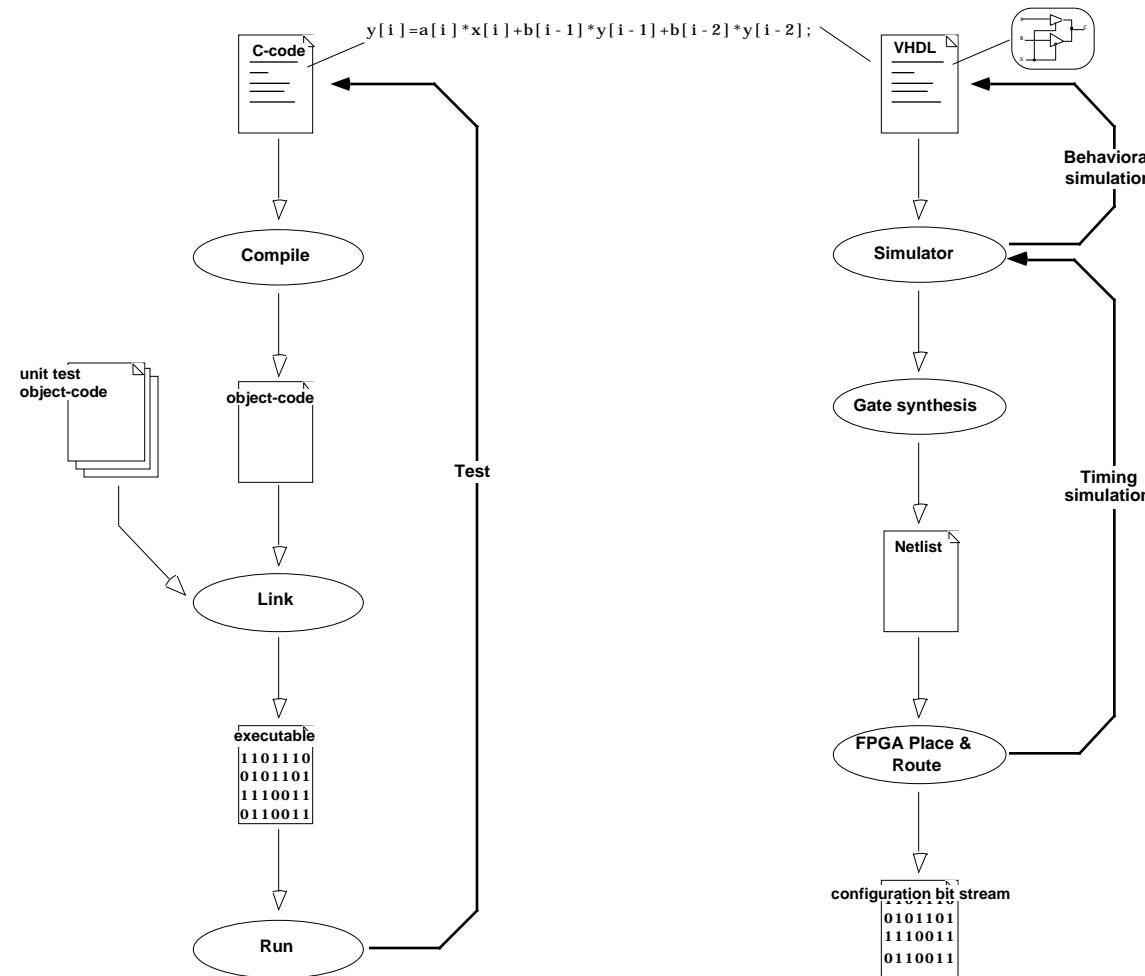
11\*3=33 cycles

3\*2=6 cycles



# FPGA Design

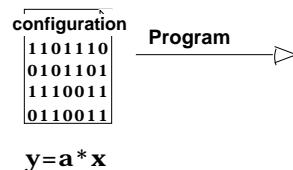
- Uses same tools as for chip design: a hardware description language (VHDL) or graphical schematic capture



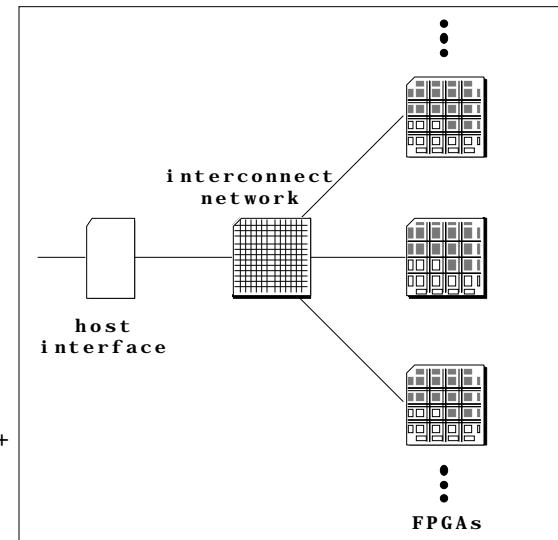
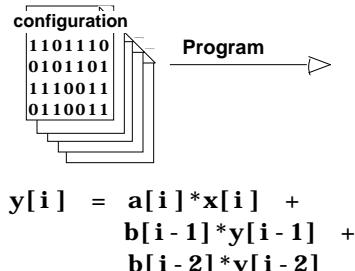
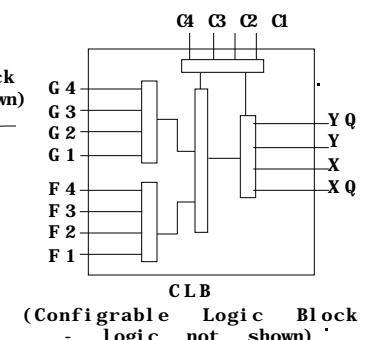
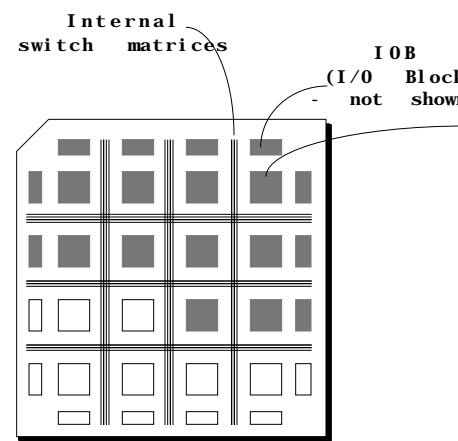


# FPGA Programming

- Programming can be done at any time during system execution
- May different types of functions can be executed by one hardware system



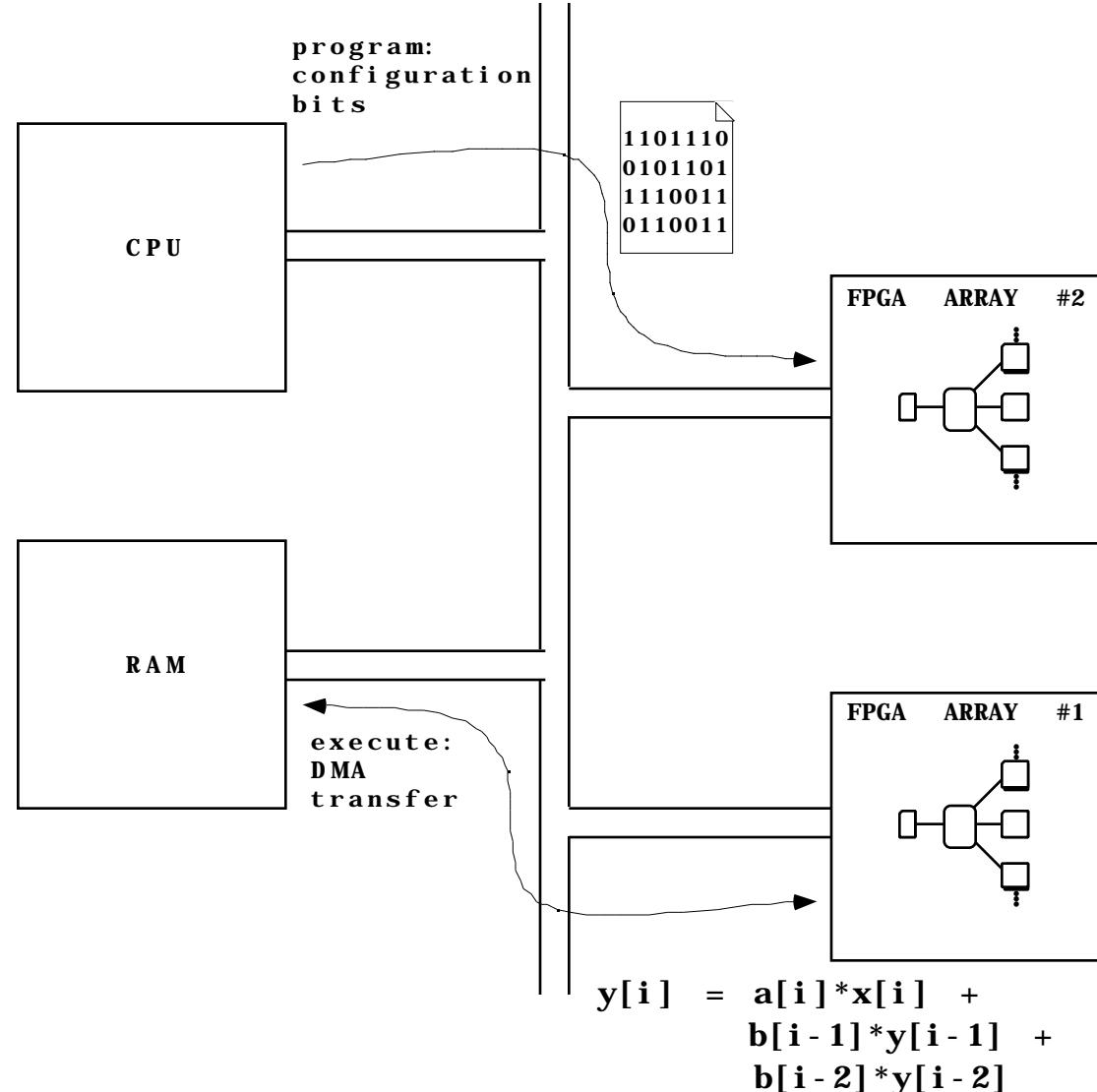
Example:  
Xilinx 4025 has 1024 CLBs & 256 I/OBs  
~30-35k gates (e.g. a 32k x 1 RAM)





# Host / FPGA Co-processor

- One possible architecture interleaves two FPGA co-processor boards: One may be programmed while the other is executing





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# Current Status

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- RTOP in initial stages of problem definition
- Will be working with AVHRR data and Code 935